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Amendment to the Claims:

Listing of Claims:

1. (Currently amended) A semiconductor component having comprising a semiconductor substrate and having an insulating layer produced on the semiconductor substrate and having a capacitance structure (K) produced in the insulating layer, which
 - [[[-]]] wherein the capacitance structure comprises has a first substructure (T1a) which has a first cohesive latticed metal region (G1a) which extends in a first common plane (M1) parallel to the substrate surface such that it has common top and bottom surfaces which limit the first cohesive latticed metal region (G1a) in each of its subregions from above and from below, and wherein the first cohesive latticed metal region (G1a) is electrically connected to a first connecting line, and
 - [[[-]]] which a first substructure has having electrically conductive regions (P1a; KN) which are arranged in the cutouts in the first cohesive latticed metal region (G1a) of the first substructure (T1a) at a distance from the edge regions of the cutouts in the common plane (M1), and wherein the electrically conductive regions (P1a; KN) are electrically connected to a second connecting line, and
characterized in that wherein the electrically conductive regions are comprise one of metal plates (P1a to P1c) or node points (KN) between via connections.
2. (Currently amended) The semiconductor component as claimed in claim 1, characterized in that wherein the capacitance structure (K) further comprises has a second substructure (T1b) which is produced parallel to and at a distance from the first substructure (T1a) and which has wherein the

second substructure comprises a metal, second cohesive latticed metal
region (G1b) which extends in a second common plane (M2) parallel to the
substrate surface such that it has common top and bottom surfaces which
limit the second latticed metal region (G1b) in each of its subregions from
above and below, and wherein the first and second substructures (T1a, T1b)
being are electrically connected.

3. (Currently amended) The semiconductor component as claimed in
claim 2, characterized in that wherein the second substructure (T1b) is of the
same design as the first substructure (T1a), and the two first and second
substructures (T1a, T1b) are arranged offset from one another such that the
electrically conductive regions (P1a) of the first substructure (T1a) are
arranged vertically above the crossing points (KP) in the second cohesive
latticed metal region (G1b) of the second substructure (T1b), and the crossing
points (KP) in the first cohesive latticed metal region (G1a) of the first
substructure (T1a) are arranged vertically above the electrically conductive
regions (P1b) of the second substructure (T1b).

4. (Currently amended) The semiconductor component as claimed in
either of claims 2 and claim 3, characterized in that wherein the crossing
points (KP) in the first cohesive latticed metal region (G1a) of the first
substructure (T1a) are electrically connected to the electrically conductive
regions (P1b) of the second substructure (T1b) which are arranged vertically
below, and the electrically conductive regions (P1a) of the first substructure
(T1a) are electrically connected to the crossing points (KP) in the second
cohesive latticed metal region (G1b) of the second substructure (T1b) which
are arranged vertically below, by means of at least one respective via
connection (V).

5. (Currently amended) The semiconductor component as claimed in claim 2, ~~characterized in that~~ wherein the second cohesive latticed metal region (G1b) of the second substructure (T1b) is offset from the first substructure (T1a), so that the electrically conductive regions (P1a) of the first substructure (T1a) are arranged vertically above the crossing points (KP) in the second cohesive latticed metal region (G1b) of the second substructure (T1b).

6. (Currently amended) The semiconductor component as claimed in claim 5, ~~characterized in that~~ wherein the electrically conductive regions (P1a) of the first substructure (T1a) and the crossing points (KP) in the second cohesive latticed metal region (G1b) of the second substructure (T1b) are electrically connected by means of one or more respective via connections (V).

7. (Currently amended) The semiconductor component as claimed in ~~one of claims~~ claim 2 to 6, characterized in that a further comprising substructure is in the form of a metal plate (MP) which is electrically connected to one of the crossing points (KP) in a latticed region (G1a; G1b) of a the first and second substructure (T1a, T1b) or to the electrically conductive regions (P1a, P1b) of the first and second substructures by means of one or more respective via connections (V).

8. (Currently amended) The semiconductor component as claimed in ~~one of the preceding claims~~ claim 1, characterized in that wherein the first cohesive latticed metal regions region (G1a to G1c) have has at least two square or round cutouts.